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DS-1PL-MS Video Motion Detection Module

Functional

The DS-1PL-MS uses the same video processing as the standalone DS-1PL but allows the user to select multiple video signals to be switched to the unit. The master is then responsible for storing the motion detection criteria from one camera to the next for true VMD processing. The DS-1PL-MS also has included activity detection for use in multiplexers in addition to the high end VMD detection.

The DS-1PL-MS architecture uses a flash CA 3306CE A/D converter that samples the video in real time and stores two successive images in two OKI M514421-30R field memories. The high performance sync stripper GS4882 guarantees quality and noise free control of all circuitry along with an AD8044AN precision video op amp for level control. The field is sampled with 7 bit resolution and 262,144 pixels per field. The A/D is controlled by a Lattice ispl1016 EPLD in conjunction with a uPD6453CY OSD controller used for multiple zone selection. The motion criteria is further processed by a high speed Dallas 87C520 along with the I2C communication to the host. This high speed pipeline processing yields an equivalent of a 52MiPs processing engine.

The host controller then can process further the VMD and Video Activity Detection (VAD) data for various functions. The VAD data can be used in determining the picture update rate of Multiplexers or Digital Video Recorders or homing a switcher to present to a guard monitor or buzzer. The host when detection of VMD on a priority camera could then route this video signal more often or constantly to the VMD module to perform more accurate detection. The host may also further process the VMD date for motion tracking, direction sensing and other high end features.

Serial Protocol

Communications

1. **I2C Bus**

1a. **Master/Slave**
The Motherboard is considered the Master (providing the clock) and the VMD is considered the Slave.

1b. **Baud Rate**

To be determined by the existing firmware on the motherboard, which presently communicates with other peripherals.
Approx. 41us clock period (13us SCL high)
Approx. 12us SDA setup, 12us SDA hold.

1c. **Addresses**

The master address is E1h (read) and E2h (write).

1d. **Termination**

The pullup resistors for SDA/SCL will be on motherboard, so the VMD module has no pullup resistors.

1e. **Communications during normal operation**

1 < Wait for BUSY to go low
2 > Send Start
3 > Send Addr Byte E2h, 8bits
4 > R/W bit low for write
5 < VMD acks
6 > Send Data command byte, 8bits
7 < VMD acks
8 > Send Stop
9 < VMD sends BUSY high for 3 frames
10 < Wait for BUSY to go low
11 > Send Start
12 > Send Addr Byte E1h, 8bits
13 > R/W bit high for read
14 < VMD acks
15 < Receive Data status byte, 8bits
16 < VMD does not ack
17 > Send Stop

2. Motherboard to DS-1PL-MS Communication

2a. **Request for motion status command:**

XD00:CCCC
Single Byte, where:
X=0 for status request (X=1 for Configure)
D=1 for day, D=0 for night
CCCC= camera number 0-15 (1-16)

2b. **Send Configuration Data to VMD:**

XDZR:CCCC, data.....
Single Byte Header, where:
X=1 for Configure
D=1 for day, D=0 for night
Z=zone pattern data
R=registers data (trig & sens & track)
CCCC= camera number 0-15 (1-16)

Registers Data:

1: Trigger Level, VMD, LSB # of pixels 0-65535 (default 500)
2: Trigger Level, VMD, MSB
*(3: Trigger Level, ACT, LSB # of pixels 0-65535 (default 5))
*(4: Trigger Level, ACT, MSB)
5: Sensitivity, VMD 0-99, (0=off 99=most sensitive),
6: Sensitivity, ACT (both default 50)
7: Tracking Time,VMD 1-99, in seconds, default 3
*(8: Tracking Time,ACT default 1))

* = defaulted by VMD module, so unimplemented

Zone Pattern Data

72 Byte stream, bit pattern interleaved between Activity Detection and Motion Detection. Represents 24 horizontal by 12 vertical zone cells. Starting from top-left, to bottom right, as in TV-type scanning. The first byte represents the top left 4 zones, with even bits (0,2,4,6) for Motion Detection, and odd bits (1,3,5,7) for Activity Detection, with least significant bits representing the left most zone cell.

Example 1: Send all night data to camera 11:

1: BAh (1011:1010) header
2: VMD Trig Lvl LSB
3: VMD Trig Lvl MSB
*(4: ACT Trig Lvl LSB)
*(5: ACT Trig Lvl MSB)
6: VMD Sensit
7: ACT Sensit
8: VMD Tracking time
*(9: ACT Tracking time)
10-81: Zone Pattern

* = defaulted by VMD module, so unimplemented

Example 2: Send day trigger/sens/track to camera 4

1: D3h (1101:0011) header
2: VMD Trig Lvl LSB
3: VMD Trig Lvl MSB
*(4: ACT Trig Lvl LSB)
*(5: ACT Trig Lvl MSB)
6: VMD Sensit
7: ACT Sensit
8: VMD Tracking time
*(9: ACT Tracking time)

* = defaulted by VMD module, so unimplemented

2c. **Request for presence/version status command:**

Done on boot, to check the presence of a VMD module in the system, and check its version.

0111:0101 75h

2d. **NTSC/PAL configure command:**

Done on boot, to configure the VMD module for NTSC or PAL video format.

0111:0000 70h NTSC
0111:0001 71h PAL

3. **DS-1-PL-MS to Motherboard Communication**

3a. **Motion Status:**

0EAM:CCCC

Single Byte, where:
E=Error (such as loss of video)
A=Activity Alarm
M=Motion Detector Alarm
CCCC= camera number 0-15 (1-16)

This status byte will be sent back on average after 3 frames (0.1s) from the time of motion status request.

3b. **Configuration Data Confirmation:**

After a block of data is sent to the VMD correctly, it will confirm with a AAh.

3c. Presence/Version Status:
After a Presence/Version request (75h) has been sent to the VMD, it will respond with:

100V:VVVV

where VVVVV is a version number 0-31.

SEQUENCE OF OPERATION

1: Motherboard to VMD:
Connect new camera to VMD from Matrix

2: Motherboard to VMD:
Send "Request for motion status" command

3: VMD to Motherboard:
Receive Motion Status Byte

4: Motherboard:
Process motion status for video routing.

5: Motherboard:
Calculate next camera for VMD, and go back to 1

DS1-PL-MS Connector
IDC-20 Pin Header

Pin#	Function:
1	+5V (pin 1 closest to corner of circuit board)
2	+5V
3	GROUND
4	GROUND
5	Video Input
6	Video Input
7	GROUND
8	GROUND
9	n/c
10	n/c
11	GROUND
12	GROUND
13	n/c
14	n/c
15	n/c
16	n/c
17	n/c
18	BUSY (busy when hi)
19	SCL (I2C)
20	SDA (I2C)